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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,790	10/19/2005	Francesco Pessolano	NL030397US1	4003
65913	7550	06/22/2009		
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER KING, JOHN B	
			ART UNIT 2435	PAPER NUMBER
			NOTIFICATION DATE 06/22/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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DETAILED ACTION

1. This office action is in response to applicant's amendment after final filed on June 11, 2009.
2. Claims 1-14 are pending in this application.
3. Applicant's arguments in respect to the issues of Claims 1-14 have been considered but they are not persuasive.

Response to Arguments

4. Applicant's arguments filed June 11, 2009 have been considered but they are not fully persuasive. In the remarks applicant argues:

I) Thuringer does not teach "pairs of processing signals coming into and out of respective ones of the processing circuits".

II) Thuringer does not teach "aspects regarding activity information derived from each pair of processing signals".

III) The combination of Thuringer and Patterson would render the invention inoperable because Thuringer is an asynchronous circuit while Patterson is a synchronous circuit.

IV) The AND gate 8 cannot correspond to both the activity monitoring circuit and the current drawing circuit.

In response to applicant's arguments:

I) Thuringer, Figure 2, teaches a set of invertors and AND gate 8 that receives the incoming signals and outputs a signal based upon the incoming signals. This monitors the state of the incoming signals and outputs a corresponding signal based upon the input signals. The claim language is broad and the examiner believes that the cited portion of Thuringer does teach this activity monitoring circuit.

II) Thuringer teaches interpreting the incoming signal as a logic high or logic low. This signal came from another part of the circuit and based upon the activity in the other part of the circuit the signal will be either a 1 or 0. This is considered as activity information. The claims just say activity information is derived, but do not go into any details about what this activity information is comprised of. Therefore, Thuringer teaches the broad claim limitations.

III) It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify an asynchronous circuit to use a clock and become a synchronous circuit. Thuringer, col. 3 lines 32-34, specifically teaches "This concept can be realized independently of the construction of the logic (synchronous or asynchronous circuit technique)."

IV) The examiner has never stated that the AND gate is both the activity monitoring circuit and the current drawing circuit. The AND gate monitors the activity of the circuit and generates the complementary information. This information is later used by the load drawing circuit of Thuringer to draw the complementary power to mask the power supply current.

Art Unit: 2435

5. The remaining arguments have been responded to previously in the previous action. Furthermore, the previous rejection of claims 1-14 still stands based upon the provided prior art and arguments as stated above.

/JBK/

/Kimyen Vu/

Supervisory Patent Examiner, Art Unit 2435